WHAT IS CLAIMED IS:

1. A processing method of supporting message signaled interrupt, applied to a chip set which is coupled to a PCI bus and a system memory, the processing method comprising at least:

monitoring a memory write transaction of the PCI bus; and

performing an interrupt sequence when an address of the memory write transaction falls into a reserved interrupt address; wherein

the reserved interrupt address is located in an address of the system memory.

2. The processing method according to claim 1, wherein the chip set is coupled to a central processing unit, and the interrupt sequence includes the following steps:

writing a system specified message of an interrupt message to the system memory according to the interrupt message of the memory write transaction;

adding an interrupt counting value after the system specified message is written into the system memory;

generating an interrupt request to the central processing unit according to the interrupt counting value; and

activating an interrupt service routine by the central processing unit.

3. The processing method according to claim 2, wherein the interrupt sequence further comprises:

reading the interrupt counting value and saving the interrupt counting value as a sent interrupt counting value;

scanning the reserved interrupt address of the system memory according to the sent interrupt counting value;

processing all the system specified messages in the reserved interrupt address, and

calculating the number of the processed system specified messages as the read interrupt counting value; and

equalizing the interrupt counting value to the interrupt counting value subtracted with the read interrupt counting value.

4. The processing method according to claim 3, wherein the step of calculating the interrupt counting value comprises:

equalizing the read interrupt counting value to the sent interrupt counting value when the read interrupt counting value is smaller than the sent counting value.

5. The processing method according to claim 2, wherein the interrupt sequence further comprises:

reading the interrupt counting value and saving the interrupt counting value as a sent interrupt counting value;

scanning the reserved interrupt address according to the sent interrupt counting value;

processing all the system specified messages in the reserved interrupt address and calculating the number of the system specified message that have been processed as the read interrupt counting value; and

equalizing the interrupt counting value to the interrupt counting value subtracted with a larger one between the read interrupt counting value and the sent interrupt counting value.

6. The processing method according to claim 2, wherein the step of writing the system specified message of the interrupt message into the system memory according to the interrupt message of the memory write transaction includes the following steps:

generating an actual memory address according to the interrupt message of the

memory write transaction; and

writing the system specified message into the actual memory address of the system memory.

7. The processing method according to claim 2, wherein the interrupt message of the memory write transaction includes a system specified address and the system specified message.

8. A message signaled interrupt controller, applied to a system that comprises a chip set, a PCI bus and a system memory, wherein the chip set is coupled to the PCI bus and the system memory and includes a dynamic random access memory controller, a CPU interface and an interrupt controller, the message signaled interrupt controller comprising:

a message signaled interrupt detector, coupled to the PCI bus and the dynamic random access memory controller to monitor a memory write transaction of the PCI bus, and when an address of the memory write transaction falls within a reserved interrupt address, a system specified message is written to the system memory via the dynamic random access memory controller and a message signaled interrupt acknowledging signal is output;

a message signaled interrupt calculator, coupled to the message signaled interrupt detector and the CPU interface to receive and count the message signaled interrupt acknowledging signal and to form an interrupt counting value, converting the interrupt counting value into a sent interrupt counting value, and outputting the sent interrupt counting value; and

a message signaled interrupt generator, coupled to the message signaled interrupt calculator and the interrupt controller, to generate a message signaled interrupt request signal to the interrupt controller, so as to enable the interrupt controller to generate an

interrupt request signal; wherein

the reserved interrupt address is located in the system memory.

9. The message signaled interrupt controller according to claim 8, wherein the chip set is further coupled to a central processing unit, and the message signaled interrupt generator is coupled to the CPU interface, after processing the system specified message, the central processing unit outputs an interrupt service termination signal to the message signaled interrupt generator and a read interrupt counting value to the message signaled interrupt calculator via the CPU interface.

10. The message signaled interrupt controller according to claim 8, wherein the chip set is coupled to a central processing unit to obtain the sent interrupt counting value via the motherboard interface.

11. The message signaled interrupt controller according to claim 8, wherein the message signaled interrupt detector generates an actual memory address according to an interrupt message of the memory write transaction, and write the system specified message of the memory write transaction into the actual memory address of the system memory via the dynamic random access memory controller.

12. The message signaled interrupt controller according to claim 8, wherein the interrupt message memory of the write transaction includes a system specified address and the system specified message.

13. A chip set of supporting message signaled interrupt, the chip set being coupled to a PCI bus, a central processing unit and a system memory, and the chip set comprising:

a dynamic random access memory controller, coupled to the system memory to control and access the system memory;

a CPU interface, coupled to the central processing unit as a control interface between the chip set and the central processing unit;

an interrupt controller, coupled to the CPU interface to generate an interrupt request signal to the central processing unit, and to enable the central processing unit to initiate an interrupt service routine; and

a message signaled interrupt controller, coupled to the PCI bus, the dynamic random access memory controller, the CPU interface and the interrupt controller to monitor a memory write transaction of the PCI bus, when an address of the memory write transaction falls into a reserved interrupt address, a system specified message is written into the system memory via the dynamic random access memory controller, and a message signaled interrupt request signal is output to enable the interrupt controller to generate the interrupt request signal; wherein

the reserved interrupt address is located in an address of the system memory.

14. The chip set according to claim 13, wherein the message signaled interrupt controller comprises:

a message signaled interrupt detector, coupled to the PCI bus and the dynamic random access memory controller to monitor the memory write transaction, and when the address specified in the interrupt message of the memory write transaction falls into the reserved interrupt address, the system specified message is written into the system memory via the dynamic random access memory controller and a message signaled interrupt acknowledging signal is output;

a message signaled interrupt calculator, coupled to the message signaled interrupt detector and the CPU interface to receive and count the message signaled interrupt acknowledging signal to form an interrupt counting value, and to convert the interrupt

counting value into a sent interrupt counting value, and to output the sent interrupt counting value according to the motherboard interface; and

a message signaled interrupt generator, coupled to the message signaled interrupt calculator and the interrupt controller, to generate the message signaled interrupt request signal to the interrupt controller according to the interrupt counting value, and to enable the interrupt controller to generate the interrupt request signal.

15. The chip set according to claim 14, wherein the message signaled interrupt generator is further coupled to the CPU interface, and after processing the system specified message, the central processing unit outputting an interrupt service termination signal to the message signaled interrupt generator and a read interrupt counting value to the message signal interrupt counter via the CPU interface.

16. The chip set according to claim 14, wherein the central processing unit obtains the sent interrupt counting value via the CPU interface.

17. The chip set according to claim 14, wherein the message signaled interrupt detector generates an actual memory address according to the interrupt message of the memory write transaction, and writes the system specified message of the memory write transaction into the actual memory address of the system memory.

18. The chip set according to claim 14, wherein the central processing unit reads sent interrupt counting value, scans the reserved interrupt address of the system memory according to the sent interrupt counting value, processes the number of all the system specified message in the reserved interrupt address as a read interrupt counting value, and outputs the read interrupt counting value.

19. The chip set according to claim 18, wherein the central processing unit determines that the read interrupt counting value is smaller than the sent interrupt

counting value, the read interrupt counting value is equal to the sent interrupt counting value.

20. The chip set according to claim 18, wherein message signaled interrupted calculator makes the interrupt counting value equal to the interrupt counting value subtracted with a larger one between the read interrupt counting value and the sent interrupt counting value.